Amendments to the Claims:

Claims 1, 6, 9, 12, 15, and 20 have been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application. Please cancel claims 23 through 46, without prejudice to the filing of one or more divisional applications including same.

Listing of Claims:

1. (Currently Amended) A semiconductor device, comprising:

a first functional die including at least a first bond pad;

at least a second functional die including at least a second bond pad, the at least a second functional die formed and coupled as a unitary integral wafer segment ~~and formed on a common semiconductor substrate~~ with the first functional die; and

an adjacent die interconnection circuit operably coupling the at least a first bond pad of the first functional die with the at least a second bond pad of the at least a second functional die.

2. (Original) The semiconductor device, as recited in claim 1, wherein the adjacent die interconnection circuit includes at least one conductor segment having a first end electrically coupled to the at least a first bond pad and a second end electrically coupled to the at least a second bond pad.

3. (Previously presented) The semiconductor device, as recited in claim 2, wherein the adjacent die interconnection circuit further includes a conductive bump electrically coupled to the at least one conductor segment configured for operatively coupling the at least one conductor segment of the semiconductor device with a substrate contact of a higher level packaging element.

4. (Original) The semiconductor device, as recited in claim 1, wherein the first functional die and the at least a second functional die are immediately adjacent.

5. (Original) The semiconductor device, as recited in claim 1, wherein the first functional die and the at least a second functional die are separated by at least one nonfunctional die.

6. (Currently Amended) The semiconductor device, as recited in claim 2, further comprising:

at least one nonfunctional die including at least one bond pad, the at least one nonfunctional die being formed on the unitary integral wafer segment ~~common semiconductor substrate~~ and located thereon adjacent to one of ~~between~~ the first functional die and the at least a second functional die; and

wherein the at least one conductor segment extends between the at least a first bond pad and the at least one bond pad of the at least one nonfunctional die, the adjacent die interconnection circuit further including a second conductive segment extending between the at least one bond pad of the at least one nonfunctional die and the at least a second bond pad.

7. (Original) The semiconductor device, as recited in claim 6, further comprising a nonfunctional die bond pad isolation conductive segment including a first end electrically attached to the at least one conductor segment and the second conductive segment for coupling the at least a first bond pad of the first functional die with the at least a second bond pad of the at least a second functional die, the nonfunctional die bond pad isolation conductive segment further including a second end extending to the at least one nonfunctional die bond pad, the nonfunctional die bond pad isolation conductive segment being fabricated as an open circuit.

8. (Original) The semiconductor device, as recited in claim 6, wherein the at least one nonfunctional die further includes an isolation device coupled to the at least one bond pad of the at least one nonfunctional die for electrically isolating the at least one nonfunctional die from the adjacent die interconnection circuit.

9. (Currently Amended) A segment of a semiconductor wafer, comprising:

two or more functional dice each including at least one bond pad, the two or more functional dice being on a unitary integral ~~semiconductor~~ wafer segment; and

an adjacent die interconnection circuit for mutually operably coupling each at least one bond pad of the two or more functional dice to at least one other bond pad of the two or more functional dice.

10. (Original) The segment of a semiconductor wafer, as recited in claim 9, wherein the adjacent die interconnection circuit couples the two or more functional dice identified by testing of the semiconductor wafer to determine an operational status of each die on the semiconductor wafer.

11. (Original) The segment of semiconductor wafer, as recited in claim 9, wherein the adjacent die interconnection circuit includes a conductor segment for coupling between each of the two or more functional dice, the conductor segment including a first end electrically coupled to the at least one bond pad on one of the two or more functional dice and a second end electrically coupled to the at least one bond pad on another of the two or more functional dice.

12. (Currently Amended) The segment of semiconductor wafer, as recited in claim 9, further comprising:

at least one nonfunctional die including at least one bond pad, the nonfunctional die being formed on the unitary ~~semiconductor~~ integral wafer segment and located thereon with the two or more functional dice; and

wherein the adjacent die interconnection circuit extends between the at least one bond pad of the at least one nonfunctional die to the at least one bond pad of the two or more functional dice.

13. (Original) The segment of semiconductor wafer, as recited in claim 9, wherein the two or more functional dice are immediately adjacent on the segment of semiconductor wafer.

14. (Original) The segment of semiconductor wafer, as recited in claim 9, wherein the two or more functional dice are separated by at least one nonfunctional die on the segment of semiconductor wafer.

15. (Currently Amended) A semiconductor wafer, comprising:

a plurality of dice each including a bond pad, the plurality of dice segregated according to functional dice and nonfunctional dice; and

an adjacent die interconnection circuit operably coupling a first bond pad of a first functional die with a second bond pad of a second functional die, the first functional die and the second functional die being on a unitary integral portion of the semiconductor wafer and further configured as an independently functional segment of the semiconductor wafer. ~~operatively adjacent.~~

16. (Previously presented) The semiconductor wafer, as recited in claim 15, wherein the first functional die and the second functional die are immediately adjacent on the semiconductor wafer.

17. (Previously presented) The semiconductor wafer, as recited in claim 15, wherein the first functional die and the second functional die are separated by at least one nonfunctional die on the semiconductor wafer.

18. (Previously presented) The semiconductor wafer, as recited in claim 15, wherein the adjacent die interconnection circuit includes at least one conductor segment having a first end electrically coupled to the first bond pad and a second end electrically coupled to the second bond pad for electrically coupling the first bond pad with the second bond pad.

19. (Previously presented) The semiconductor wafer, as recited in claim 18, wherein the adjacent die interconnection circuit further includes a conductive bump electrically coupled to the at least one conductor segment configured for operatively coupling the at least one conductor

segment of the semiconductor wafer with a contact of a higher level packaging.

20. (Currently Amended) The semiconductor wafer, as recited in claim 18, further comprising:

at least one nonfunctional die including at least one bond pad, the nonfunctional die being formed on the unitary integral wafer segment ~~a common semiconductor substrate~~ and located thereon adjacent to one of ~~between~~ the first functional die and the second functional die; and

wherein the at least one conductor segment extends between the first bond pad and the at least one bond pad of the at least one nonfunctional die, the adjacent die interconnection circuit further including a second conductive segment extending between the at least one bond pad of the at least one nonfunctional die and the second bond pad.

21. (Previously presented) The semiconductor wafer, as recited in claim 20, further comprising a nonfunctional die bond pad isolation conductive segment including a first end electrically attached to the at least one conductor segment and the second conductive segment for coupling the first bond pad of the first functional die with the second bond pad of the second functional die, the nonfunctional die bond pad isolation conductive segment further including a second end extending to the at least one bond pad of the nonfunctional die, the nonfunctional die bond pad isolation conductive segment being fabricated as an open circuit.

22. (Original) The semiconductor wafer, as recited in claim 20, wherein the at least one nonfunctional die further includes an isolation device coupled to the at least one bond pad of the at least one nonfunctional die for electrically isolating the at least one nonfunctional die from the adjacent die interconnection circuit.

Claims 23-46 (Canceled)